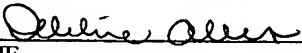


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APPLICATION FOR LETTERS PATENT

FOR

LDMOS TRANSISTOR

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LDMOS TRANSISTOR

FIELD OF THE INVENTION

The present application relates to an LDMOS transistor structure.

5 BACKGROUND OF THE INVENTION

LDMOS transistor structures are widely used as semiconductor devices for many types of transistor applications such as high voltage MOS field effect transistors. An LDMOS transistor comprises a lightly doped drain region to enhance the breakdown voltage. LDMOS transistors comprise, thus, a higher on resistance due
10 to the lightly doped region within the drain. The interrelation between breakdown voltage and on-resistance relates to the maximum electric field defined by the pn-junction which needs to stay below the critical electric field for the semiconductor to avoid breakdown. This maximum electrical field is defined by the doping level of, for example, the n^- doped drain in a nmos field effect transistor. Furthermore, in
15 applications in which the transistor is most of the time driven to conduct, the long on-state can lead to substantial hot carrier injection resulting in DC parametric drift. This is a very common issue with LDMOS transistor structures.

Fig. 1 shows a typical power LDMOS transistor. A wafer comprises, for example, a p substrate 13 on top of which an epitaxial layer 1 is deposited. This
20 layer 1 includes n conductivity type areas 2 and 4, 15 implanted into the surface to provide a source and drain region, respectively. The epitaxial layer 1 is usually covered with an insulating dielectric layer 7 such as silicon oxide in which a polysilicium gate 8 is arranged to cover the channel between the drain 4, 15 and source 2. The drain in this exemplary LDMOS transistor comprises a first region
25 which is n^+ doped and which comprises a connection to a drain electrode 12 arranged above that region 15 through a window in the insulator layer 7. This n^+ region is surrounded by a lighter doped n^- region 4 that extends until under gate 8 to define a channel between the source and the drain region. On the source side of this transistor

a p^+ doped sinker 14 is provided which extends from the surface of the epitaxial layer 1 down to the substrate to provide for a backside source contact. Contact 11 connects the source region 2 with the sinker 14.

Fig. 2 shows an LDMOS transistor as proposed for use, for example, in smart power applications. A wafer comprises, for example, a p substrate 1 which includes n conductivity type areas 2 and 4, 6 diffused or implanted into the surface to provide a source and drain region, respectively. The substrate 1 is usually covered with an insulator layer 7 such as silicon oxide in which a polysilicium gate 8 is arranged to cover the channel between the drain 4, 6 and source 2. The drain in this exemplary LDMOS transistor comprises a first region 6 which is n^+ doped and which comprises a connection to a drain electrode 10 arranged above that region 6 through a window in the insulator layer 7. From this n^+ region extends a lighter doped n^- region 4 to the left of region 6 until under gate 8 to define a conducting path to the gate channel region. To extend the field effect pinch-off depletion zones from above, a layer of p material 5 is implanted in the upper part of the extended region 4 of the drain and reaching the top surface of the epitaxial layer.

SUMMARY OF THE INVENTION

According to the present application, a new transistor structure is introduced. For example, a semiconductor transistor structure comprises a substrate having an epitaxial layer of a first conductivity type, a source region extending from the surface of the epitaxial layer of a second conductivity type, a drain region within the epitaxial layer of a second conductivity type, a channel located between the drain and source regions, and a gate arranged above the channel. The drain region may comprise a first region of the second conductivity type for establishing a contact with an electrode, a second region of the second conductivity type being less doped than the first region being buried within the epitaxial layer and extending from the first region horizontally in direction towards the gate, a third region being of the second conductivity type less doped than the second region and extending vertically from the

surface of the epitaxial layer and horizontally from the second region until under the gate, a top layer of the first conductivity type extending from the surface of the epitaxial layer to the second region, and a bottom layer of the first conductivity type extending from the second region into the epitaxial layer.

5 The third region may comprise a first sub-region of the second conductivity type extending from the second region horizontally towards the gate and a second sub-region of the second conductivity type extending vertically from the surface of the epitaxial layer and horizontally from the first sub-region until under the gate. The first sub-region may be less doped than said second region and the second
10 sub-region being less doped than the first sub-region. Alternatively, the first sub-region can be less doped than that second region and the first and the second sub-region may overlap and the first sub-region can be partially less doped than the second sub-region. The semiconductor structure may further comprise a voltage termination of the second conductivity type extending from the electrode deeper into the epitaxial
15 layer than the first region. The semiconductor structure may also further comprise a sinker structure of the first conductivity type extending from the source region to the bottom of the epitaxial layer. The substrate can be heavily doped. The second region can have an approximate horizontal length of 1- 3 microns. The first conductivity type can be a p-type and the second conductivity type can be an n-type or vice versa.

20 Another embodiment is a semiconductor transistor structure comprising a substrate having an epitaxial layer of a first conductivity type, a source region extending from the surface of the epitaxial layer of a second conductivity type, a drain region within the epitaxial layer of a second conductivity type, a channel located between the drain and source regions, and a gate arranged above the channel. The
25 drain region may comprise a first region of the second conductivity type for establishing a contact with an electrode, a second region of the second conductivity type being less doped than the first region being buried within the epitaxial layer and extending from the first region horizontally in direction towards the gate, a third

region of the second conductivity type being less doped than that second region and extending from the second region horizontally towards the gate, a fourth region of the second conductivity type being less doped than the third region and extending vertically from the surface of the epitaxial layer and horizontally from the third region
5 until under the gate, a top layer of the first conductivity type extending from the surface of the epitaxial layer to the second region, and a bottom layer of the first conductivity type extending from the second region into the epitaxial layer.

This semiconductor structure may further comprise a voltage termination of the second conductivity type extending from the electrode deeper into
10 the epitaxial layer than the first region. The semiconductor structure may also further comprise a sinker structure of the first conductivity type extending from the source region to the bottom of the epitaxial layer. The substrate can be heavily doped. The second region can have an approximate horizontal length of 1- 3 microns. The first conductivity type can be a p-type and the second conductivity type can be an n-type or
15 vice versa.

Yet another embodiment is a semiconductor transistor structure comprising a substrate having an epitaxial layer of a first conductivity type, a source region extending from the surface of the epitaxial layer of a second conductivity type, a drain region within the epitaxial layer of a second conductivity type, a channel
20 located between the drain and source regions, and a gate arranged above the channel. The drain region may comprises a first region of the second conductivity type for establishing a contact with an electrode, a second region of the second conductivity type being less doped than the first region being at least partially buried within the epitaxial layer and extending from the first region horizontally until under the gate, a
25 top layer of the first conductivity type extending from the surface of the epitaxial layer to the second region, and a bottom layer of the first conductivity type extending from the second region into the epitaxial layer.

This semiconductor structure may further comprise a voltage termination of the second conductivity type located on the side of the drain region opposite the side facing the gate and extending from the surface of the epitaxial layer. The semiconductor structure may also further comprise a sinker structure of the first conductivity type extending from the source region to the bottom of the epitaxial layer. The substrate may be heavily doped. The second region can have an approximate horizontal length of 1- 3 microns. The first conductivity type can be a p-type and the second conductivity type can be an n-type or vice versa.

Yet another embodiment is a semiconductor transistor structure comprising a substrate having an epitaxial layer of a first conductivity type, a source region extending from the surface of the epitaxial layer of a second conductivity type, a drain region within the epitaxial layer of a second conductivity type, a channel located between the drain and source regions, and a gate arranged above the channel. The drain region may comprise a first region of the second conductivity type for establishing a contact with an electrode, a second region of the second conductivity type being less doped than the first region being buried within the epitaxial layer and extending from the first region horizontally in direction towards the gate, a third region of the second conductivity type being less doped than that second region and extending from the second region horizontally towards the gate, a fourth region of the second conductivity type extending vertically from the surface of the epitaxial layer and horizontally from the third region until under the gate, wherein the third region and the fourth region overlap and the overlap is higher doped than the fourth region, a top layer of the first conductivity type extending from the surface of the epitaxial layer to the second region, and a bottom layer of the first conductivity type extending from the second region into the epitaxial layer.

This semiconductor structure may further comprise a voltage termination of the second conductivity type extending from the electrode deeper into the epitaxial layer than the first region. The semiconductor structure may also further

comprising a sinker structure of the first conductivity type extending from the source region to the bottom of the epitaxial layer. The substrate can be heavily doped. The second region can have an approximate horizontal length of 1- 3 microns. The first conductivity type can be a p-type and the second conductivity type can be an n-type or
5 vice versa. The third region can be partially less doped than the fourth region.

Other technical advantages of the present disclosure will be readily apparent to one skilled in the art from the following figures, descriptions, and claims. Various embodiments of the present application obtain only a subset of the advantages set forth. No one advantage is critical to the embodiments.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

A more complete understanding of the present disclosure and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

15 **Figure 1** is a partial sectional view of a semiconductor wafer including a transistor structure according to the prior art;

Figure 2 is a partial sectional view of a semiconductor wafer including a transistor structure as proposed for use for instance in smart power applications according to the prior art;

20 **Figure 3** is a partial sectional view of a semiconductor wafer including a transistor structure according to one embodiment of the present invention;

Figure 4 is a partial sectional view of a semiconductor wafer including a transistor structure according to another embodiment of the present invention;

25 **Figure 5** is a partial sectional view of a semiconductor wafer including a transistor structure according to yet another embodiment of the present invention;

Figure 6 shows graphs from a process simulation of a transistor structure according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning to the drawings, exemplary embodiments of the present application will now be described. Figure 3 depicts an improved transistor structure according to an exemplary embodiment of the present invention. On top of a p⁺ substrate 20, a p epitaxial layer 21 is arranged. For example, the substrate can be doped heavily with 10¹⁹/cm³ and the epitaxial layer can be less doped with 10¹⁵/cm³. Along the top surface of the epitaxial layer 21, a source region 23 extends laterally from the source side of gate 26 to an electrically floating electrode or metal interconnection 24. The electrically floating contact 24 connects the oppositely doped source region 23 and a p⁺ sinker region 22. The p⁺ sinker region 22 reaches from the source region 23 to the p⁺ substrate 20. A source metal contact (not shown) is placed along the entire backside of the wafer. Again an insulator layer 25 is placed on the top surface of the epitaxial layer 21 and comprises a gate 26 and windows for respective drain and source electrodes 24, 34. On top of the insulator layer 25, usually a passivation layer (not shown) is deposited.

The improved transistor structure comprises a drain region with a multiple layer arrangement as shown in Fig. 3. In this exemplary embodiment, a graded superjunction is created by this multilayer structure. A first relatively short resulting region 33 being n⁻ doped extends from under gate 26 to the drain contact electrode 34. Between this short n⁻ doped region 33 and the drain contact electrode 34 follows a second n⁻ doped region 32 which extends deeper into the epitaxial layer 21. In one embodiment, a graded doping concentration from region 33 to region 28 with increasing doping concentration is obtained. However, other embodiments are possible. In one preferred embodiment, the maximum doping concentration of this region 32 is not necessarily higher than the maximum doping concentration for region 33. The implant dose of region 32 could be less than that of region 33. However, the region 32 implant overlaps with the region 33 implant and is partially compensated by the region 31 implant. The doping overlap between regions 32 and 33 results in a higher doping concentration in the part of the overlap region of 32 as compared to the

region 33 and a lower doping concentration in the remaining part of region 32. This is because the doping concentration of region 33 drops with vertical distance from the top surface. Region 32, in this particular embodiment has, thus, two functions. The overlapping part of region 32 is used to carry the current whereas the lesser doped part of that region is used to relax the electrical field. Thus, different graded junctions from region 33 to region 30 can be formed which still are within the scope of the present application.

Furthermore in this embodiment, region 32 does not reach the surface of the epitaxial layer 21. However, depending on the doping concentration, this layer could also reach to the top surface of epitaxial layer 21. Between the second n^- doped region 32 and the drain contact electrode 34 extends a relatively long (appr. 1 - 3 microns) n doped conducting stripe 30 which couples the n^- doped region 32 with a heavily doped n^+ region 28 that extends from drain electrode 34 into the epitaxial layer 21. Thus, the drain starts with a heavily doped n^+ region 28 from the electrode 34 that gradually ends in a lightly doped n^- region 33 under the gate 26. The n doped conducting stripe may have an approximate horizontal length of 1- 3 microns and is basically shielded by an implanted p doped top layer 31 and bottom layer 29 that extend from the heavily n^+ doped region 28 horizontally towards gate 26 for substantially the length of the n doped conducting layer 30. In the center of the drain region starting under the drain electrode 34 a n^+ doped termination region 27 is implanted which reaches from the surface deep into the epitaxial layer 21. Region 28 is higher doped than region 27. Also, region 27 is higher doped than region 29. This is necessary to avoid breakdown between the drain contact 34 and region 29.

The lowly doped n^- region 33 close to gate 26 keeps the electric field low to suppress hot carrier injection into the gate and also to avoid early breakdown of the structure. Furthermore, this region 33 keeps the feedback capacitance C_{dg} between the gate and the drain low. The second or intermediate n^- doped region 32 can be provided for trade-off between on-resistance, breakdown of the transistor

structure, hot carrier injection, and feedback capacitance C_{dg} . The intermediate n^- doped implant region 32 can be produced, for example, through a 0 degree off-set implant mask or a tilted angle self-aligned implant mask. Such a structure with vertically alternating layers 31, 30, 29 and the graded regions 33, 32, 28 and 27 forms
5 a new combination of superjunctions and graded junctions which are used to overcome the above mentioned trade-off. The advantage with this concept lies in the fact that the highly doped conducting layer is depleted from both top and bottom, thus, also enabling a high breakdown voltage despite the higher doping concentration of the n conducting stripe. By the introduction of laterally graded junctions 33, 32, and 29
10 close to the gate 26, an optimization of several critical parameters affecting radio frequency performance is made possible. In addition to optimization of on-resistance and breakdown voltage, the graded junctions keep the electric field low at the gate oxide to suppress hot carrier injection (low drift), which as mentioned above is an important issue for LDMOS transistors. Moreover, the critical feedback capacitance
15 C_{dg} can be kept at a low value. On the right side, a deep high energy implant 27 prevents breakdown to occur between the drain contact 34 and region 29.

All regions can be created by ion implantation. The n conducting stripe can be created as a buried layer and is being depleted from the top and the bottom through layers 31 and 29, respectively. In particular implanted p layer 29 depletes the
20 n conducting stripe 30 from the bottom which makes it possible to increase the doping concentration of the n conducting stripe compared to a structure as shown in figure 2 where most of the depletion is induced from the top p layer. The top p layer 31 depletes the n conducting stripe from above in a similar way as the structure shown in figure 2. There is a lowly doped n^- region 33 close to the gate oxide 26 to keep the
25 electric field low around this critical 'corner'. This suppresses hot carrier injection into the gate oxide 26, avoids early breakdown and keeps the feedback capacitance C_{dg} low. The intermediate doped n^- implanted region 32 serves as an overlapping region between the n^- region 33 and the n conducting stripe 30. The depth and doping concentration of this implant is used to optimize the trade-off between on-resistance,

breakdown voltage, hot carrier injection and feedback capacitance C_{dg} . However, also a single n^- region 40 can be used as shown in Figure 4. Figure 4 shows only the relevant section around the gate of another exemplary embodiment which is different from the embodiment shown in Figure 3. Similar structures are designated with similar numerals.

Figure 5 shows yet another embodiment according to the present invention. Again, similar structures are designated with similar numerals. In this embodiment, regions 40 and region 30 as shown in Figure 4 are merged into a single region 50. Thus, conducting stripe 50 is practically extended to reach under gate 26. Therefore, this embodiment only provides for two grade steps in forming a graded junction, namely, the higher doped region 28 and the lower doped region 50.

However, in all embodiments, there can be two implants under the drain contact electrode 34 as shown in Figure 3. One shallow highly doped implant 28 for low contact resistance at the drain contact electrode 34 and another high energy implant 27 serving as voltage termination to prevent breakdown between the drain electrode 34 and the superjunction layer 29.

Fig. 6 shows the implemented structure as a result from process simulation in a commercial tool. The right figure shows the net doping concentration along a cutline across the superjunction stack; lateral extension of the new drain engineering is approximately $3\text{ }\mu\text{m}$. Thus, exemplary dimensions can be seen in this figure.

Although particular embodiments of the invention have been shown and described, the invention is not limited to the preferred embodiments and it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention, which is defined only by the appended claims and their equivalents. For example, the substrate can be a p-type or an

n-type substrate. Thus, source and drain region would be either of the n-type or the p-type, respectively.